

## 100V N-Channel MOSFET

### DESCRIPTION

The 100N10 uses advanced trench technology and design to provide excellent  $R_{DS(on)}$  with low gate charge. It can be used in a wide variety of applications.

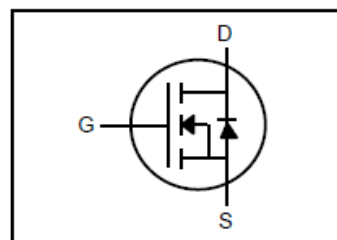
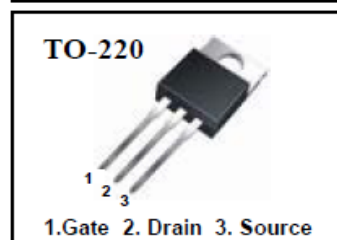
### GENERAL FEATURES

- $V_{DS} = 100V, I_D = 100A$   
 $R_{DS(on)} < 13m\Omega @ V_{GS}=10V$  (Typ:9.9m $\Omega$ )
- Special process technology for high ESD capability
- High density cell design for ultra low  $R_{dson}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

$BV_{DSS} = 100 V$   
 $R_{DS(on) typ} = 9.9 m\Omega$   
 $I_D = 100 A$



### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	100	A
Drain Current-Continuous( $T_C=100^\circ C$ )	$I_D(100^\circ C)$	80	A
Pulsed Drain Current	$I_{DM}$	380	A
Maximum Power Dissipation	$P_D$	200	W
Derating factor		1.33	W/°C
Single pulse avalanche energy (Note 5)	$E_{AS}$	800	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	°C

## Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	0.75	$^{\circ}C/W$
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## Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

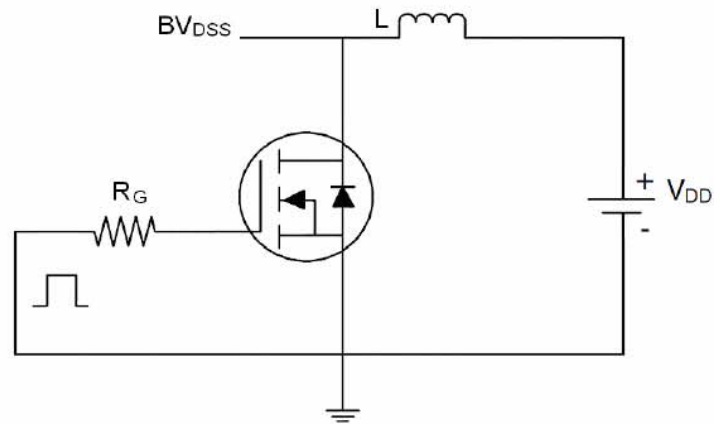
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A$	-	9.9	13	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=50V, I_D=40A$	100	-	-	S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	4800	-	PF
Output Capacitance	$C_{oss}$		-	340	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	150	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=40A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	-	15	-	nS
Turn-on Rise Time	$t_r$		-	50	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	40	-	nS
Turn-Off Fall Time	$t_f$		-	55	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=80V, I_D=40A,$ $V_{GS}=10V$	-	85	-	nC
Gate-Source Charge	$Q_{gs}$		-	18	-	nC
Gate-Drain Charge	$Q_{gd}$		-	28	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
Diode Forward Current (Note 2)	$I_S$	-	-	-	57	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}C, I_F = 40A$ $di/dt = 100A/\mu s$ (Note3)	-	38	80	nS
Reverse Recovery Charge	$Q_{rr}$		-	53	100	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

## Notes:

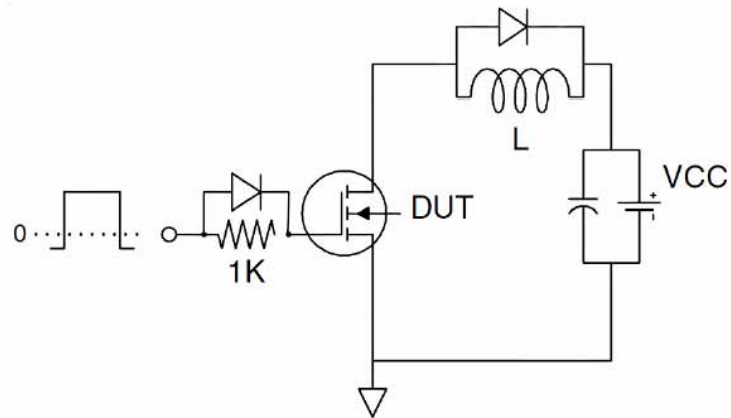
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

## Test circuit

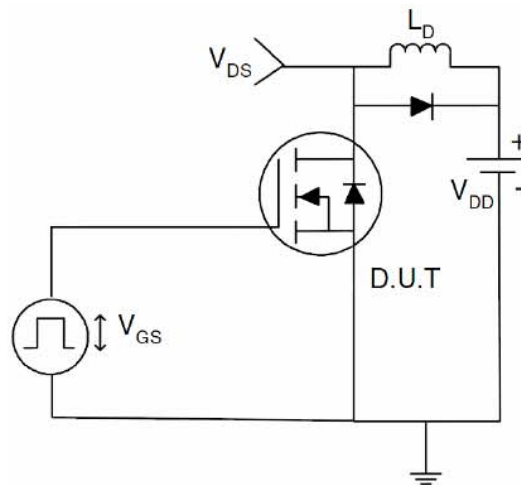
### 1) $E_{AS}$ test Circuits



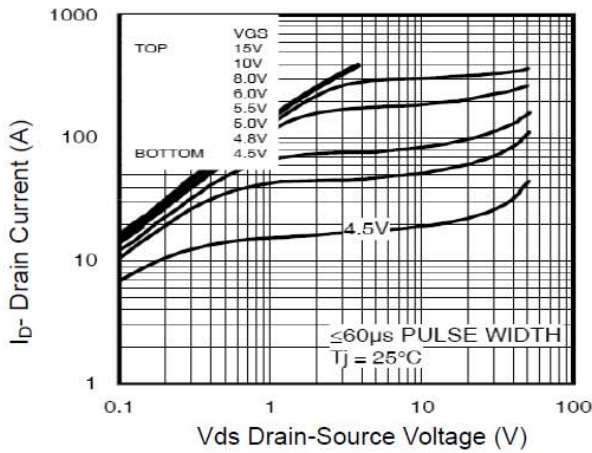
### 2) Gate charge test Circuit:



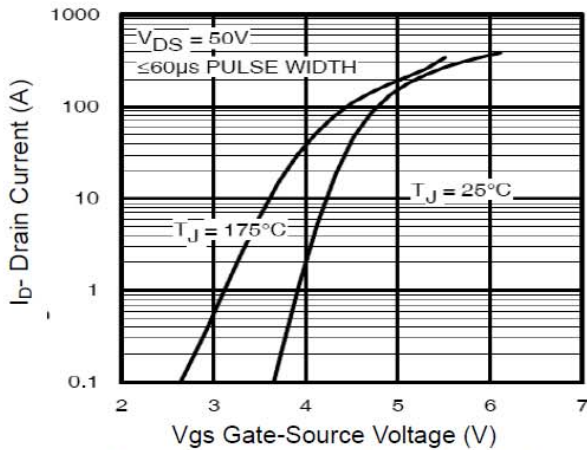
### 3) Switch Time Test Circuit:



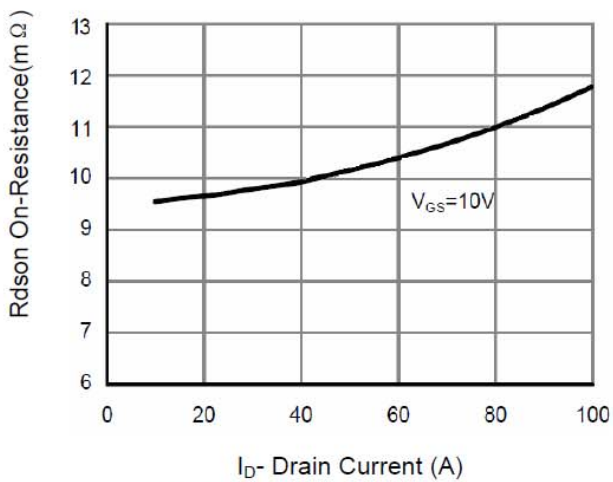
## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)



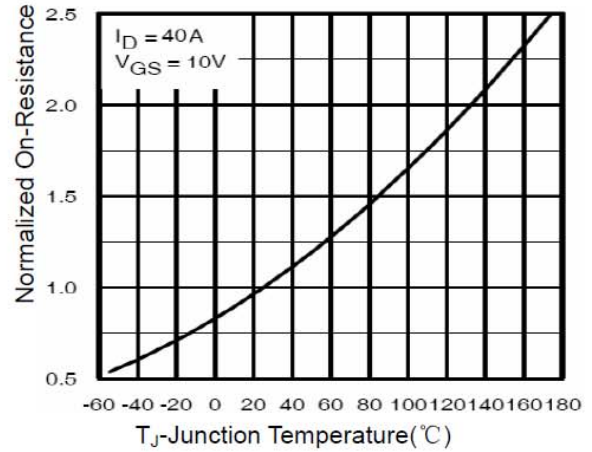
**Figure 1 Output Characteristics**



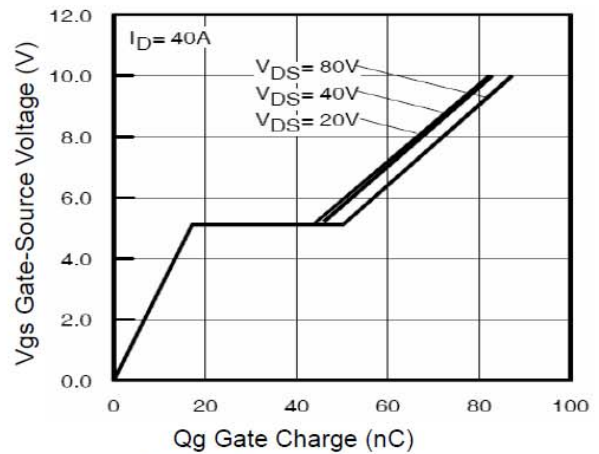
**Figure 2 Transfer Characteristics**



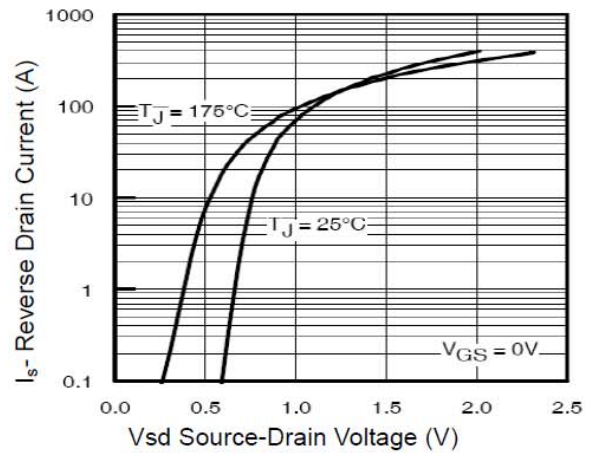
**Figure 3 Rdson- Drain Current**



**Figure 4 Rdson-Junction Temperature**

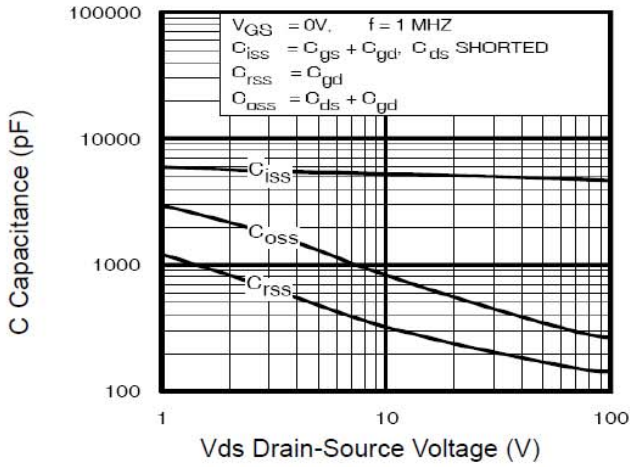


**Figure 5 Gate Charge**

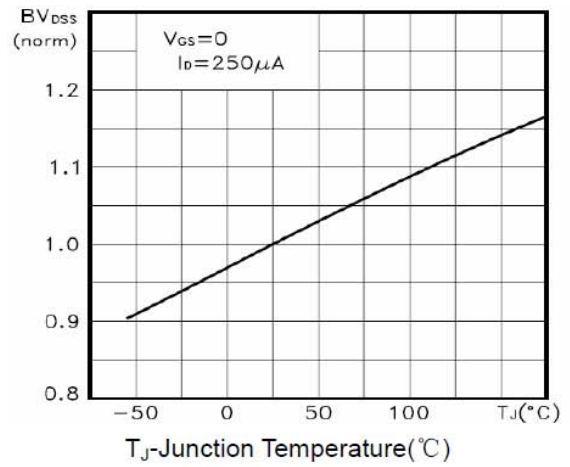


**Figure 6 Source- Drain Diode Forward**

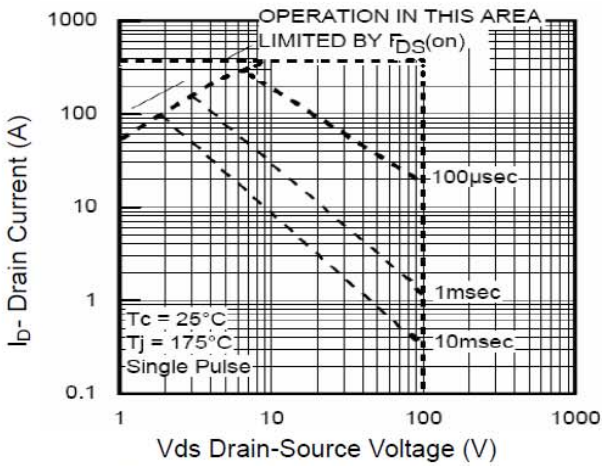




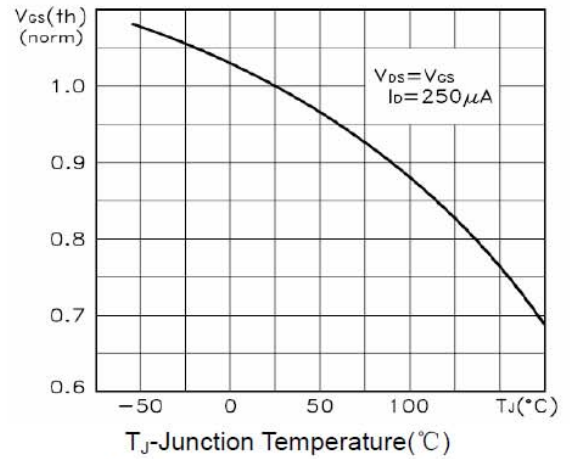
**Figure 7 Capacitance vs Vds**



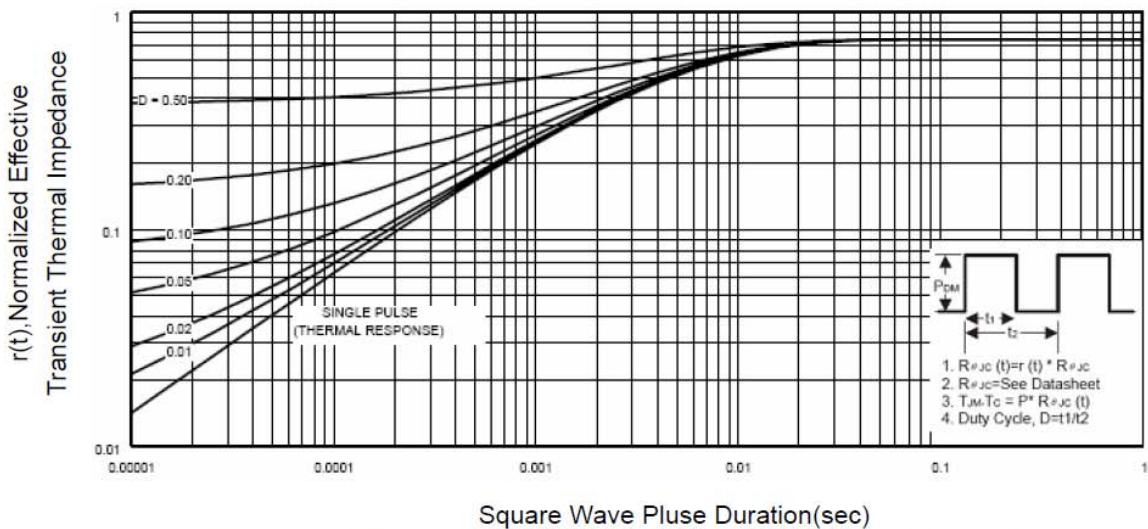
**Figure 9  $BV_{DSS}$  vs Junction Temperature**



**Figure 8 Safe Operation Area**



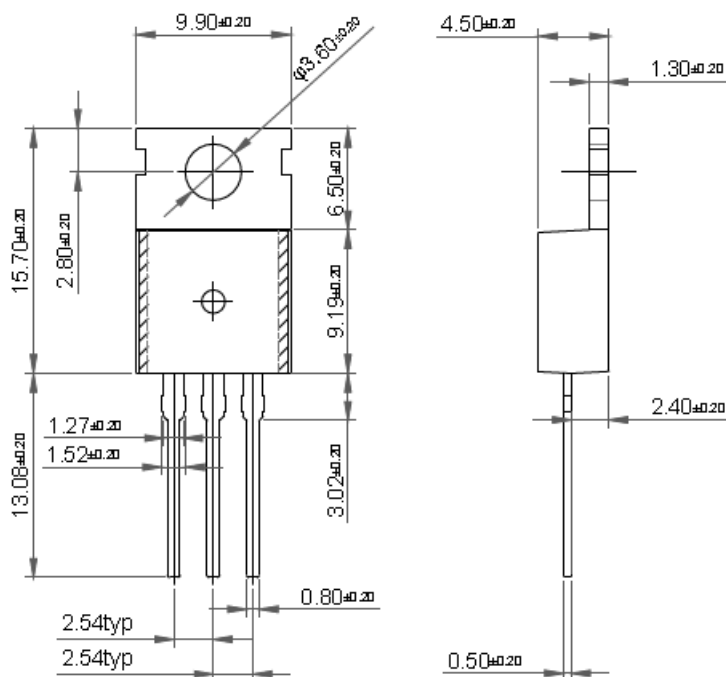
**Figure 10  $V_{GS(th)}$  vs Junction Temperature**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

## Package Dimension

### TO-220 (A)



### TO-220 (B)

